IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Eric M. Dowling	§	Group Art Unit: 2183
Serial No.: 10/074,779	§	Examiner: Huisman, David J.
Filed: February 13, 2002	§	
For: Embedded DRAM-DSP Architecture	§	Atty Docket: MICS:0171-2 1998-0010.02

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April 30, 2007 — Jeanna Reed
Date — Jeanna Reed

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

In accordance with the Official Gazette Notice of July 12, 2005, Appellant respectfully submits this Pre-Appeal Brief Request for Review. This Request is being filed concurrently with a Notice of Appeal. In the Final Office Action Mailed January 30, 2007, the Examiner rejected claims 1-14, 16-32 and 34-50. For at least the reasons set forth below, Appellant respectfully submits that the pending claims are allowable in their present form.

Rejections under 35 U.S.C § 103

The Examiner rejected claims 1, 6-10, 12-14, 23-25 and 46-48 under 35 U.S.C. § 103(a) as being unpatentable over Inagami et al., U.S. Pat. No. 4,881,168 ("the Inagami reference"), and, in addition, Wright, et al., U.S. Pat. No. 5,587,961 ("the Wright reference") was cited by the Examiner as extrinsic evidence. The Examiner also rejected claims 2-5, 11 and 26-27 under 35 U.S.C. § 103(a) as being unpatentable over the Inagami reference in view of Parady, U.S. Pat. No. 5,933,627 ("the Parady reference"), and rejected claims 16-22, 28-32, 34-45 and 49-50 under 35 U.S.C. § 103(a) as being unpatentable over the Inagami reference in view of the Parady reference and further in view of Bissett et al., U.S. Pat. No. 5,896,523 ("the Bissett reference"). Appellant respectfully traverses these rejections.

Embodiments of the present technique are directed to methods and processors that utilized an embedded DRAM processor architecture with a program-controlled data transfer and caching structure that reduces or eliminates waiting time due to DRAM accessing. *See* Specification, page 4, lines 19-21. Specifically, each of the independent claims recite an embedded DRAM processor, or a method of utilizing an embedded DRAM processor, that includes, in relevant part, "an *embedded DRAM array*." (Emphasis added). Moreover, the claimed processors and/or methods also generally recite commands (or steps) for controlling the transfer of data between the DRAM array and the register files. By way of example, independent claims 1, 13, 46 and 48 generally recite separate commands to precharge a row of DRAM, deactivate the precharged row and/or load elements (or columns) into one or more sets of data registers.

The cited references do not disclose an embedded DRAM array as recited in independent claims 1, 13, 16, 23, 28, 45, 46, 48, 49 and 50.

First, Appellant respectfully submits that the Inagami reference does not disclose an embedded DRAM array, as recited in independent claims 1, 13, 16, 23, 28, 45, 46, 48, 49 and 50. As clearly evident from Appellant's specification, an *embedded DRAM array* is a DRAM array that is *integrated onto the same chip with the processor*. *See* Specification, page 2, line 25 to page 3, line 10; page 27, line 7-8; FIG. 1. In contrast, while the Inagami reference does disclose a vector processor having a main storage 1, the main storage 1 is not integrated onto the same chip with the vector processor. *See* Inagami, col. 4, lines 15-17; FIG. 1. Indeed, nowhere does the Inagami reference disclose or suggest that the main storage 1 would be on chip with the processor and, thus, embedded with the vector processor. As such, the Inagami reference clearly does not teach the claimed embedded DRAM array.

With respect to Appellant's assertion that an "embedded DRAM array" is a DRAM array that is integrated onto the same chip as the processor, the Examiner noted that he "was unable to find an explicit definition in the specification as to what an embedded DRAM processor constitutes." Advisory Action Mailed 4/17/07, page 2. Appellant respectfully notes that to be his own lexicographer, an explicit definition in the specification need not be provided. *See* M.P.E.P. § 2111.01.IV. Rather, the Manual of Patent Examining Procedure clearly provides as follows:

> The specification should also be relied on for more than just explicit lexicography or clear disavowal of claim scope to determine the meaning of a claim term when applicant acts as his or her own lexicographer; the meaning of *a particular claim term may be defined by implication, that is, according to the usage of the term in the context in the specification.*
>
> *Id.* (Emphasis added).

Accordingly, in the context of the specification, Appellant respectfully submits that the term "embedded DRAM array" refers to DRAM that is integrated onto the same chip as the processor. Indeed, the background section of the specification describes several problems associated with accessing off-chip DRAM, such as requiring larger on-chip SRAM to avoid memory delays. *See* Specification, page 2, lines 8-24. To alleviate certain of these problems, the specification provides that DRAM may be placed onto the same chip as the processor. *See id.* page 2, lines 25-26. However, the background section describes prior art memory hierarchies as insufficient for use with this on-chip (i.e., embedded) DRAM. *See id.* page 3, lines 7-30. Further, in the detailed description section of the specification, an embedded DRAM architecture is described with the DRAM arrays 102 integrated onto the same chip as the high-speed register files 112, 114 and 116. *See id.* page 22, lines 7-9; page 23, lines 3-5; page 27, lines 7-8; FIG. 1. For instance, the external interface 130 moves data on and off of the chip containing the DRAM arrays 102, the high-speed register files 112, 114, and 116 and the functional units 128. *See id.* page 27, lines 7-8; FIG. 1. Accordingly, the specification makes clear that the term "embedded" refers to the integration of the DRAM array *onto* the same chip as the processor.

The Examiner, however, has interpreted the term "embedded DRAM array" in a manner that is improper and that is inconsistent with the specification. Indeed, the Examiner has given an interpretation to the term "embedded DRAM array" that essentially reads the term "embedded" out of the claims. In particular, the Examiner is asserting that a DRAM array is embedded in a processor when it is an integral part of the processor. In relevant part, the Examiner stated:

> Dictionary.com defines "embedded" in the following way: "To cause to be integral part of a surrounding whole." Clearly, in Fig. 1 of Inagami, the memory is an integral part of the overall processing system (processor). Hence, Inagami teaches an embedded DRAM processor.
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> Office Action Mailed April 5, 2006, page 46.

However, the Examiner's interpretation would essentially read the term "embedded" out of the present claims because any memory that is present in a processing system would necessarily be an "integral part" of that processor. Assuming the Examiner's interpretation is correct, any reference that discloses a processor that includes a DRAM array would anticipate the present claims, which require an embedded DRAM array. This is improper. Appellant's claims are directed to a processor that comprises a DRAM array. Clearly, the DRAM array is an integral part of the processor or otherwise the DRAM array would serve no purpose. In the present claims, Appellant's have chosen to further recite that the DRAM array is "embedded." The Examiner must give this term weight in the interpretation of the present claims. As described above, in the context of the specification, the term "embedded" clearly refers to the integration of the DRAM array *onto* the same chip as the processor.

Appellant therefore asserts that the Examiner's interpretation of an "embedded DRAM array" as memory that is an integral part of a processor is improper and is not the interpretation one of ordinary skill in the art would reach when reading the claims in view of the specification. Rather, as described above, one of ordinary skill in the art would understand that an "embedded DRAM array" refers to a DRAM array that is integrated onto the same chip as the processor. As the Inagami reference does not disclose a DRAM array that is integrated onto the same chip as the processor, it does not disclose each and every recitation of the present claims.

Accordingly, the Inagami reference does not disclose each and every feature recited in the present independent claims. Further, the secondary references relied on by the Examiner do not remedy the deficiencies of the Inagami reference. As such, whether taken alone or in hypothetical combination, the cited references do not render obvious the present independent claims and the claims dependent therefrom.

The cited references do not disclose separate commands to precharge, deactivate and/or load as generally recited in independent claims 1, 13, 46 and 48.

Furthermore, Appellant submits that the Inagami reference does not disclose an instruction set that includes separate commands to precharge a row of DRAM, deactivate the precharged row and/or load elements (or columns) of the precharged rows into one or more sets of data registers, as generally recited in independent claims 1, 13, 46 and 48. Indeed, the

Examiner admits that the Inagami reference is devoid of any disclosure of these recited commands. *See* Final Office Action, Mailed 1/30/2007, page 4. The Examiner, however, is asserting that the recited precharging, deactivating and loading commands are inherently disclosed by the Inagami reference. As evidence that precharge and deactivate commands exist, the Examiner cited the Wright reference. *See id.* at page 2.

To the extent that the Examiner relies on a theory of inherency, the extrinsic evidence must make clear that the missing descriptive matter is *necessarily* present in the thing described in the reference. M.P.E.P. § 2112.IV. However, contrary to the Examiner's assertions, Appellant respectfully submits that it is not necessarily true that the recited precharging, deactivating and loading would require separate commands. Indeed, the Wright reference relied on by the Examiner for support of this inherency argument makes clear that separate commands are not required. By way of example, the Wright reference contrasts synchronous DRAM (SDRAM) with asynchronous DRAM, in that SDRAM requires separate commands for precharging and accessing a row of storage cells while asynchronous DRAM does not require separate commands. *See* Wright, col. 1, lines 36-45. Therefore, separate commands for precharging, deactivating and loading are *clearly* not inherent in the Inagami reference since this feature is not necessarily present in Inagami, as the Wright reference provides at least one example of asynchronous DRAM that does not require such separate commands.

Accordingly, for this additional reason, the Inagami reference does not render obvious independent claims 1, 13, 46 and 48 and the claims dependent therefrom.

Respectfully submitted,

Date: April 30, 2007

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